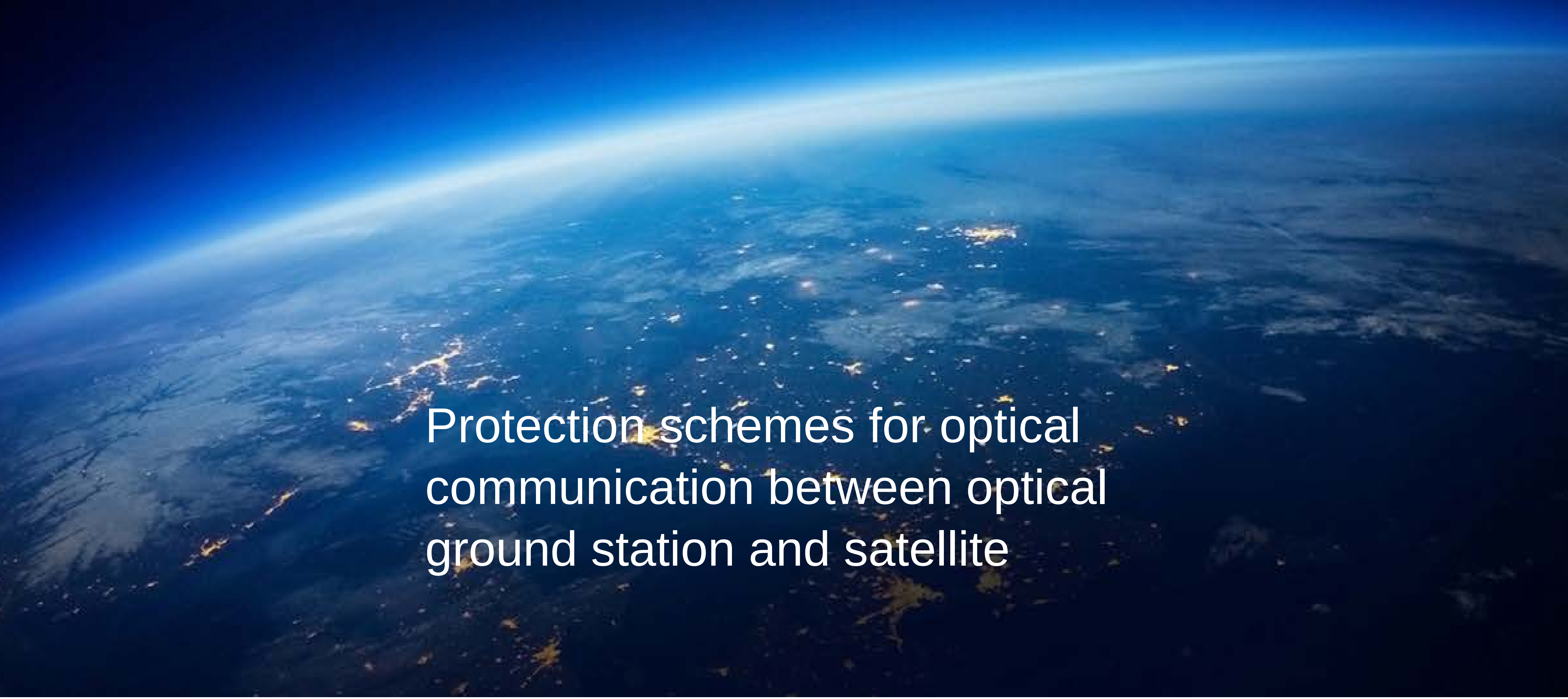
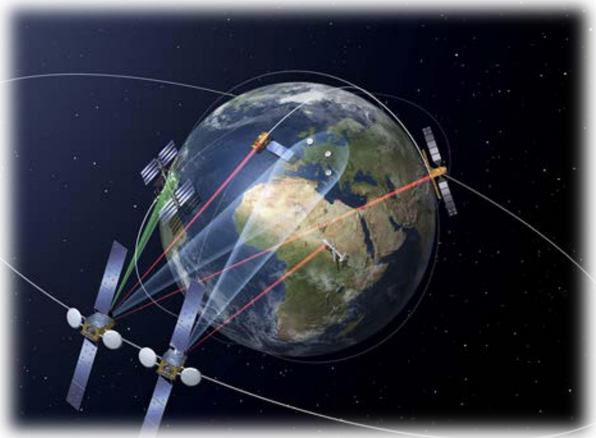


Protection schemes for optical communication between optical ground station and satellite

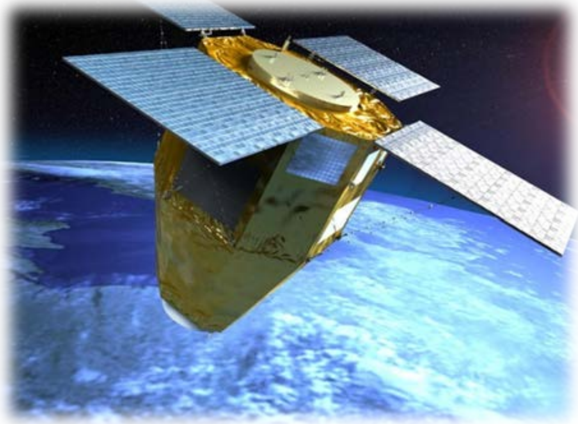
DEFENCE AND SPACE
Sylvain Poulenard
sylvain.poulenard@airbus.com
Airbus DS Toulouse

AIRBUS

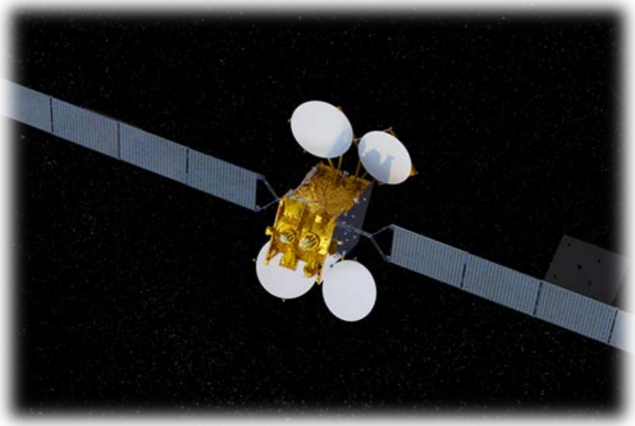
Missions



The Space Data Highway



Earth Observation LEO



Broadband satellite

Mega constellation

Optical links through the atmosphere are of interest

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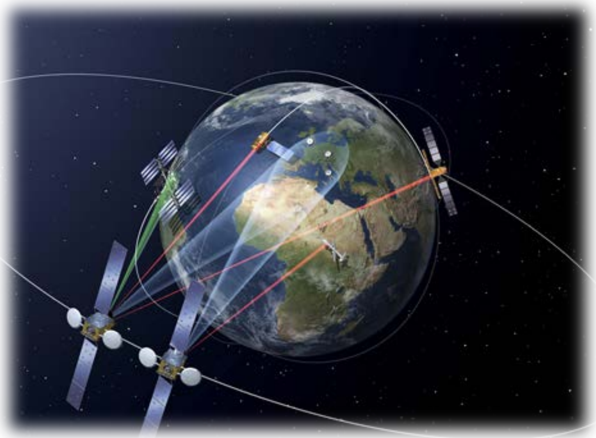
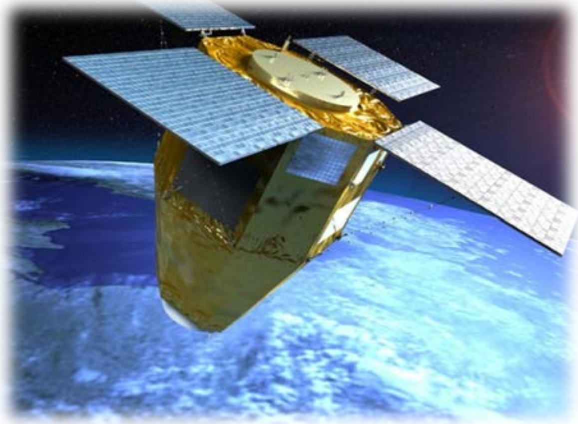
Missions – typical metrics



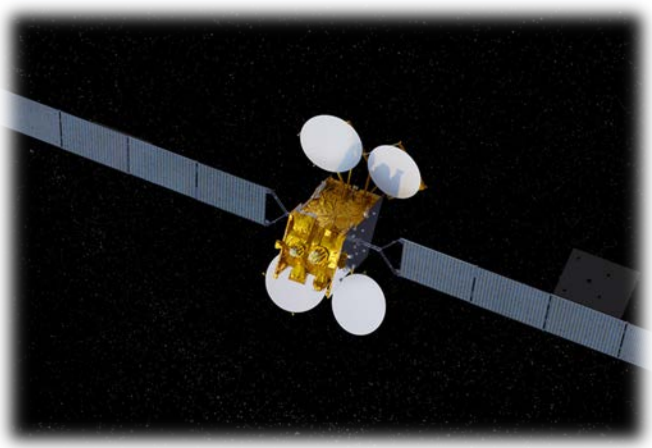
The Space Data Highway



Earth Observation LEO

Volume of images succesfully downloaded [Tbit/day]

Latency [min - hours]



Broadband satellite

Satellite capacity [Gbps – Tbps]
Services availability [99.9%]

Latency [ms – s]

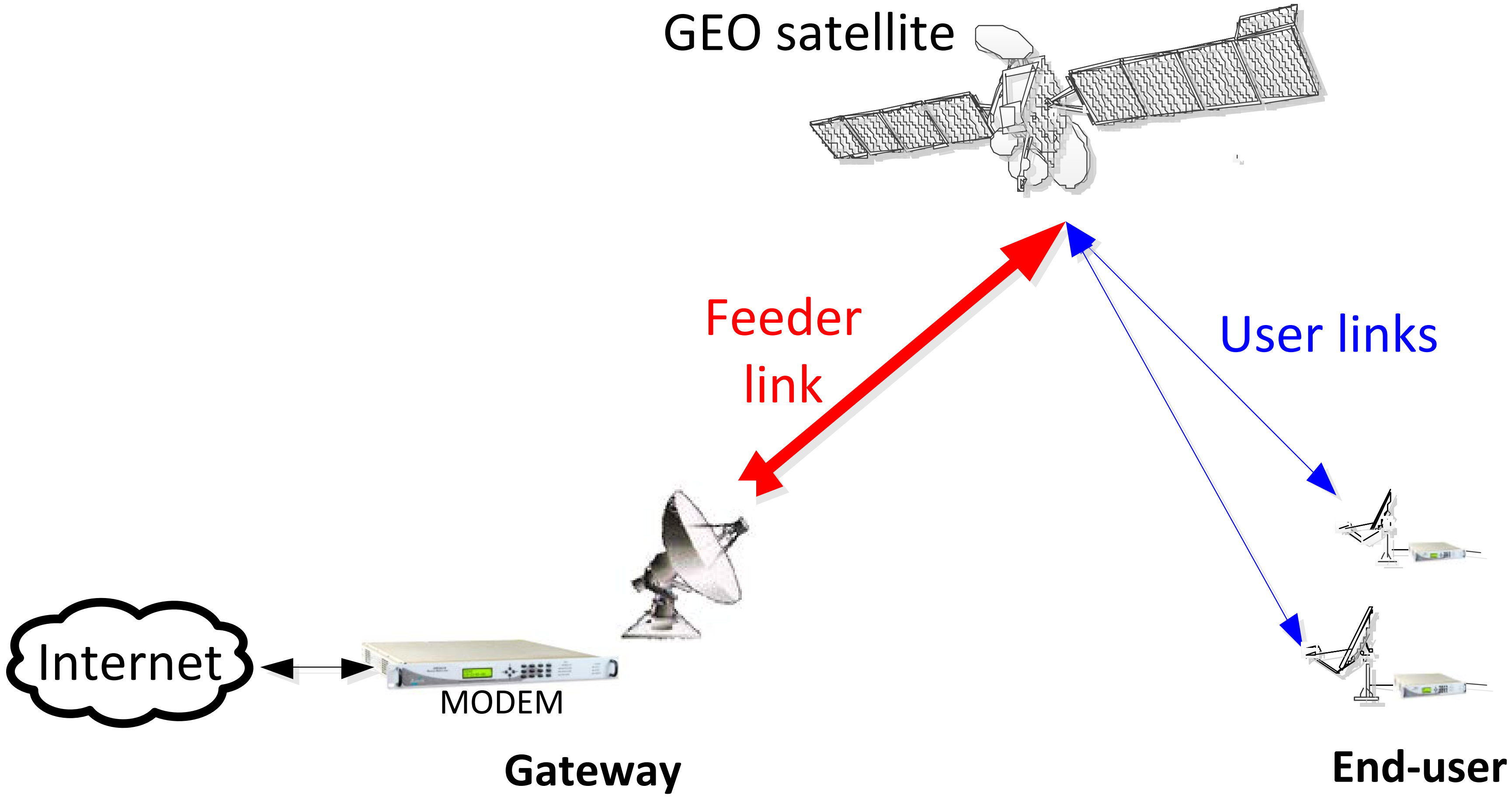
Mega constellation

Satellite capacity [Gbps – Tbps]
Services availability [99.9%]

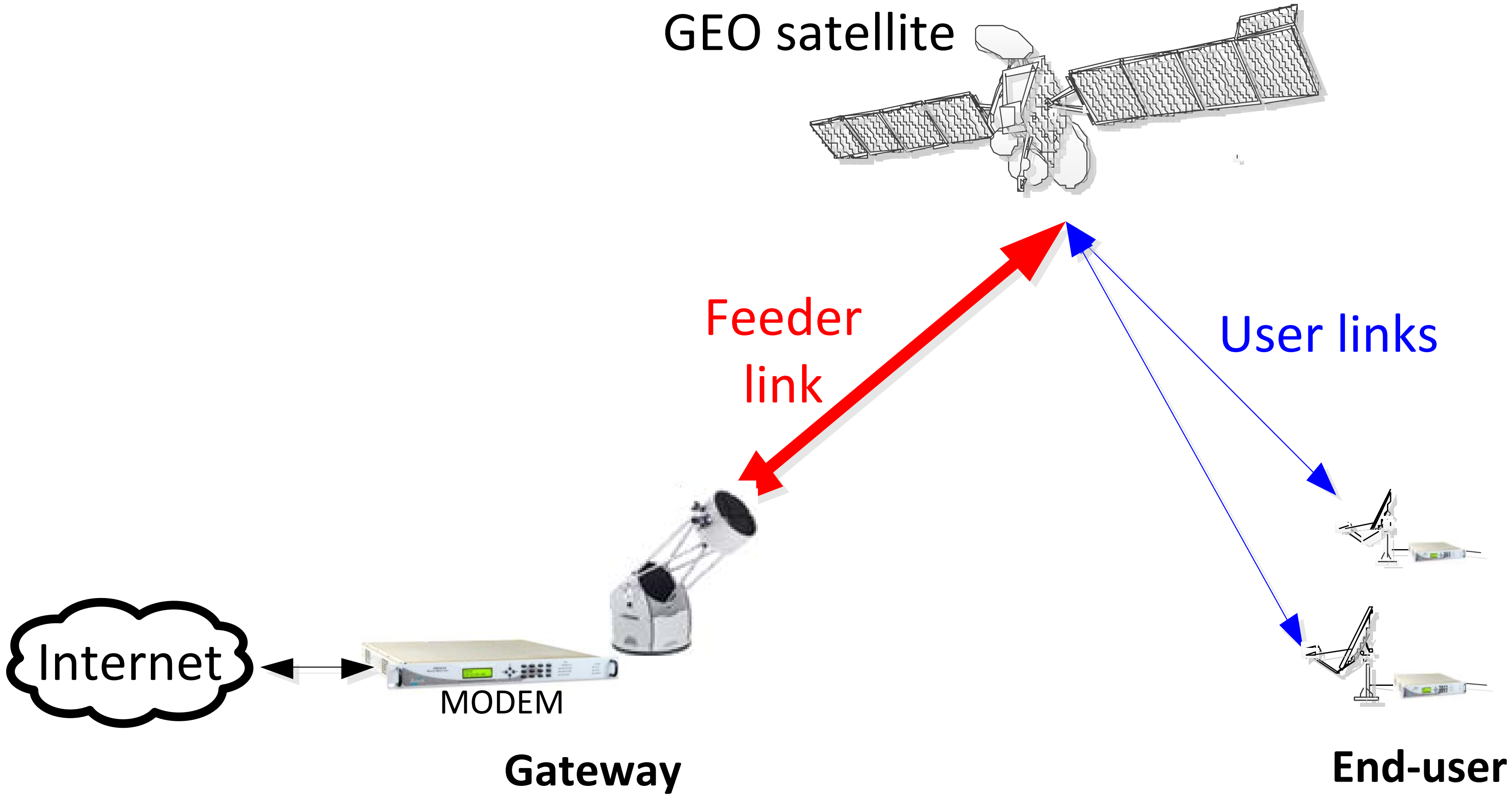
Latency [ms – s]

Atmosphere turbulence strenght is a concern

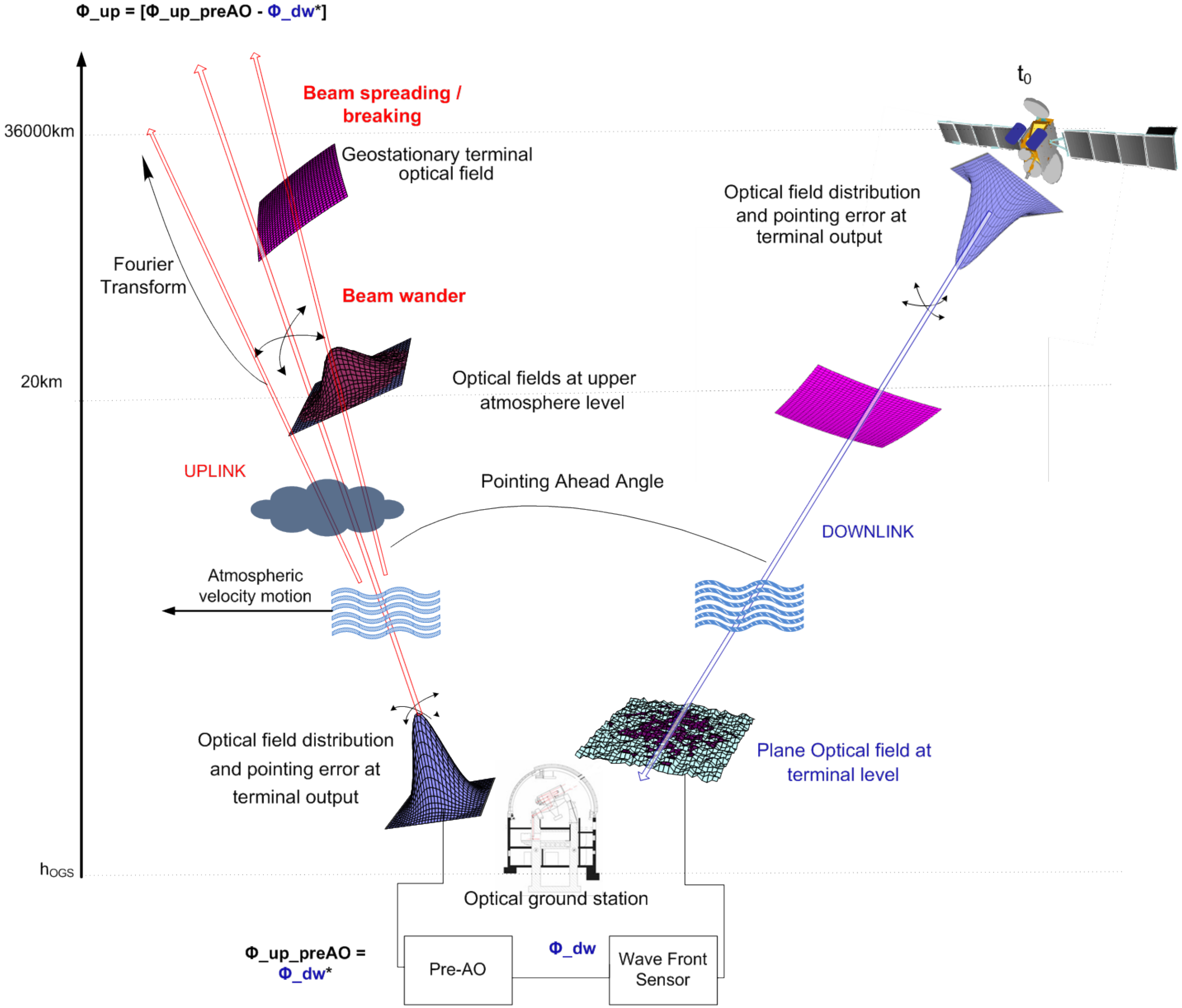
AIRBUS - feeder links



Optical feeder links



Difference between uplink and downlink



Uplink is the most demanding link

How to guaranty « availability » of a service ensured by optical links through turbulence?

Lack of Cn^2 profile retrieval for long period

➔ Definition of a « representative worst case » at Tenerife for in-orbit demonstration of optical feeder link

Availability	Nominal	« worst case »
	12cm	4cm

$\boldsymbol{r_0}$@1,55µm@zenith angle

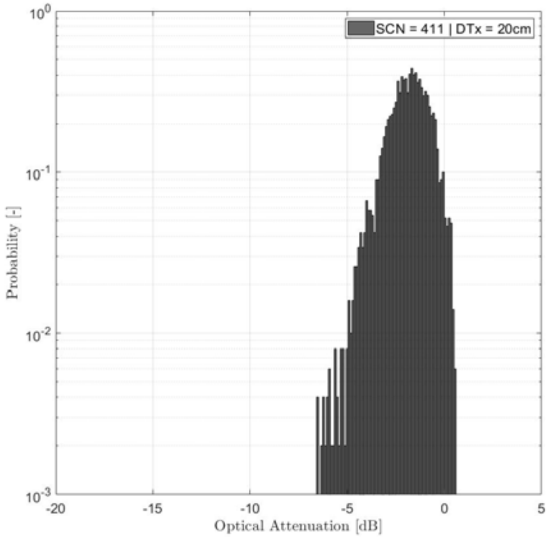
Availability	Nominal	« worst case »
	26µrad	11µrad

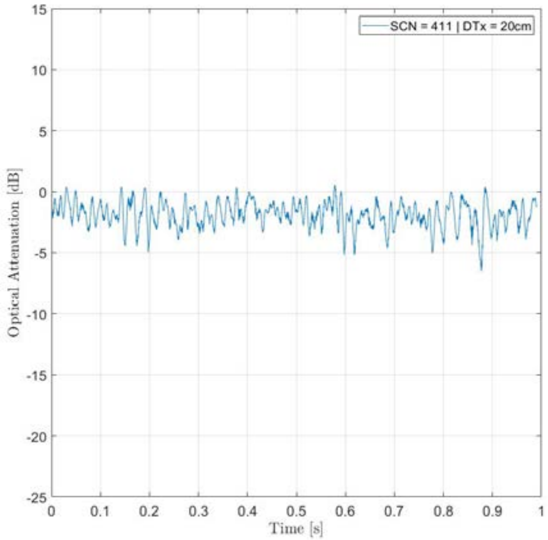
$\boldsymbol{\theta_0}$@1,55µm@zenith angle

Osborn, J., Wilson, et al. ***Optical turbulence profiling with Stereo-SCIDAR for VLT and ELT*****. Monthly Notices of the Royal Astronomical Society, 478(1), 825-834 (2018).**

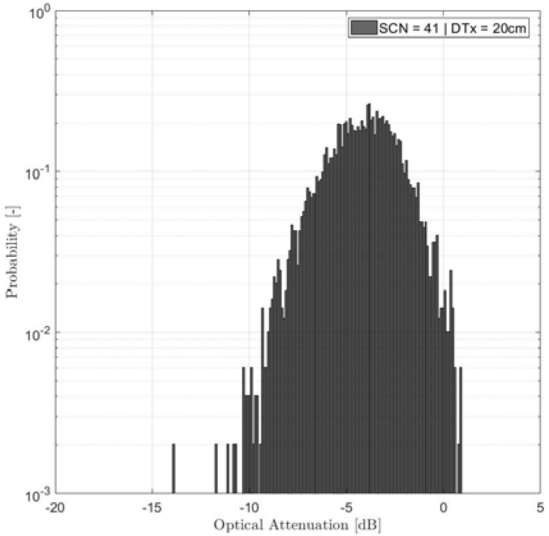
How to guaranty « availability » of a service ensured by optical uplink?

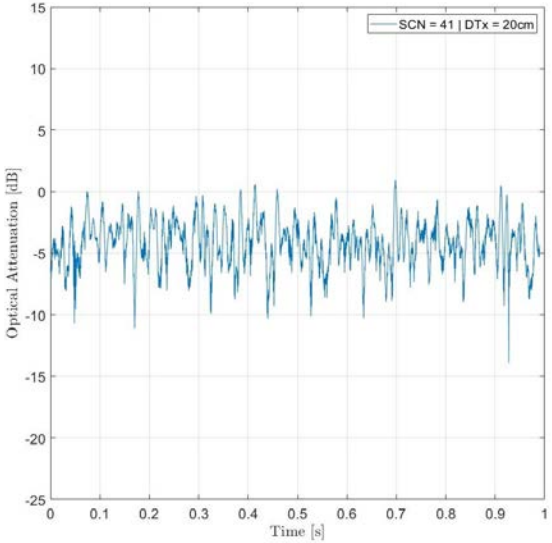
70% of the time it should be like this or better…





Some time it could be like this or worst…



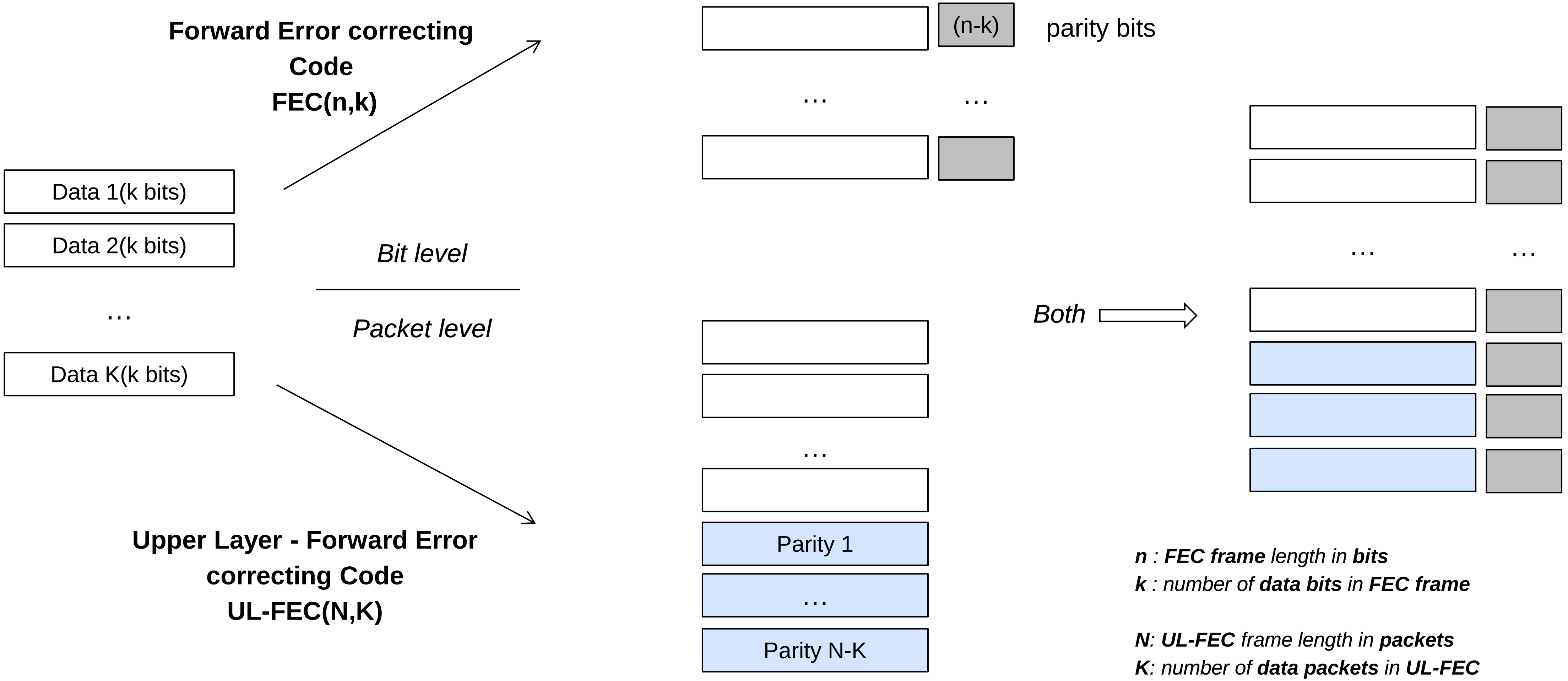


** Simulations performed by ONERA-DOTA*

In any case, it is a slow fading channel

Protection schemes

FEC to correct errors / UL-FEC to correct burst of errors



n *:* ***FEC frame*** *length in* ***bits***
k *: number of* ***data bits*** *in* ***FEC frame***

N*:* ***UL-FEC*** *frame length in* ***packets***
K*: number of* ***data packets*** *in* ***UL-FEC***

(n-k): parity to retrieve informations

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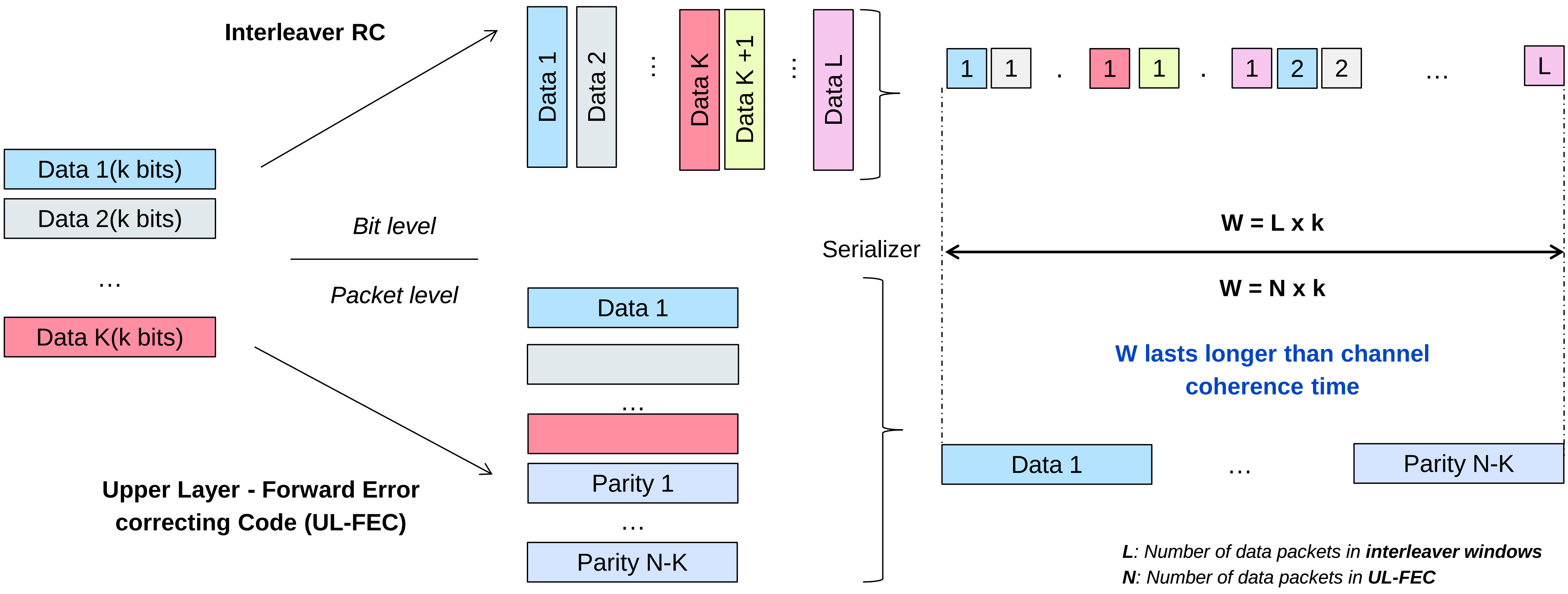
Interleaver and/or UL-FEC to get back channel diversity



W: time duration windows to get back channel diversity

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What does a good protection scheme mean for us?

✓ **Good performances and scalable**

- Low latency
- Great power saving on the link budget while maintining a high information rate
- Able to adapt to atmospheric turbulence strenght variation

✓ **Low on board resources consumption**

- Limited number of decoding iterations and simple decoding algorithms
- Easy encoding algorithms
- High level of parallelism

For low latency and high code rate {FEC + physical layer bit interleaver} is the selected option

Part 1 – 10Gbit/s downlink

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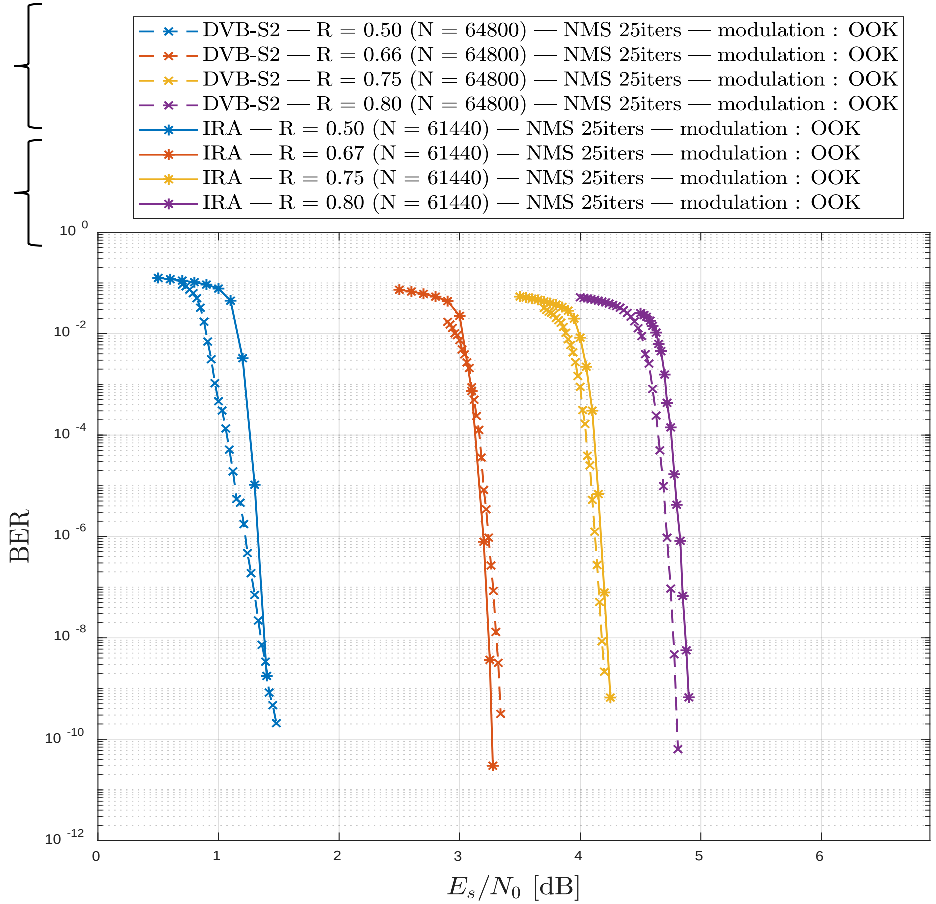
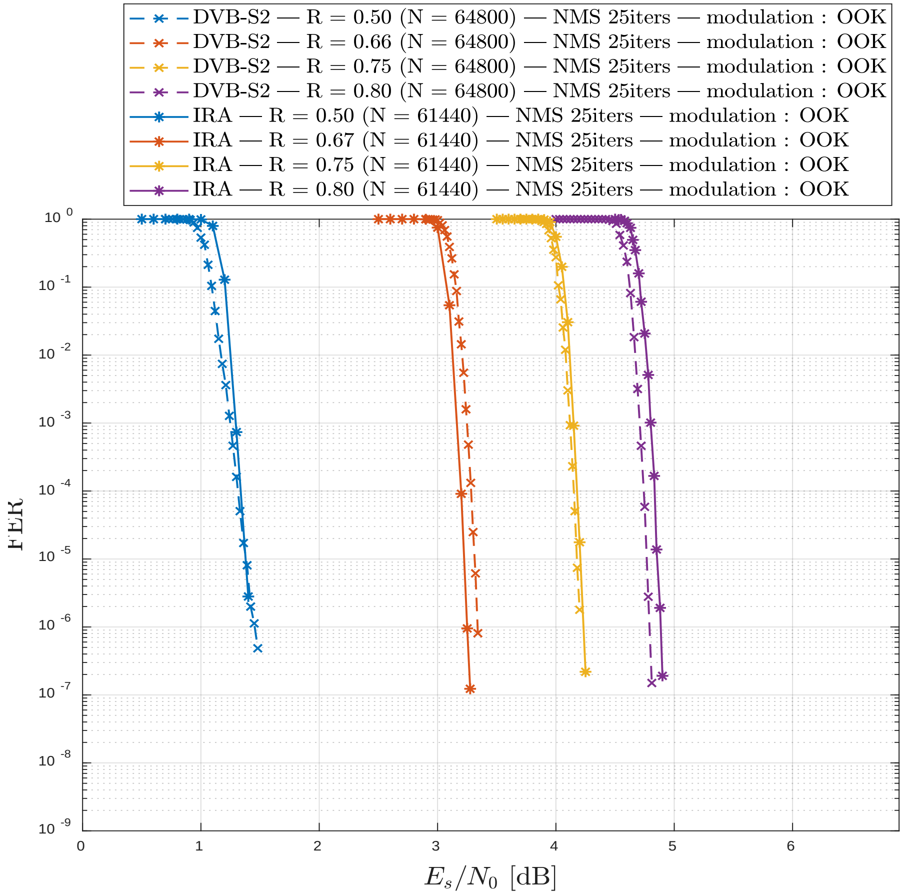
Low on board resources consumption

In-house design LDPC assuming soft inputs (Analog to digital converters)

Standard codes for RF feeder links

Codes proposed for optical feeder downlinks





With such codes a 10Gbits encoded DPSK downlink at 30° elevation should be error free under « strong » turbulence with a 4/5 FEC rate an interleaver and a < 5W optical amplifier

Good performances and scalable

In-house design LDPC assuming soft inputs (Analog to digital converters)

Generic IP core available

XILINX ALL PROGRAMMABLE.

LDPC Encoder/Decoder v2.0

LDPC Encoder/Decoder v2.0 — LogiCORE IP Product Brief

Introduction

The Low Density Parity Check (LDPC) soft IP core supports LDPC decoding and encoding. The LDPC codes used are highly configurable, and the specific code used can be specified on a codeword-by-codeword basis.

Additional Documentation

A product guide is available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/ldpc-enc-dec.html

Features

- LDPC decode or encode of a range of customer specified Quasi-cyclic (QC) codes, including 5G NR codes
- Throughput[1] up to:
  - 1.78 Gb/s for LDPC decode @ 8 iterations
  - 12.5 Gb/s for LDPC encode
- High bandwidth AXI4-Stream interfaces

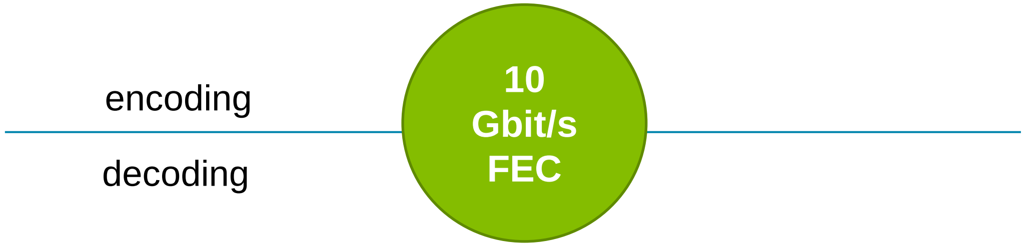
1. See performance in the Product Guide for clock frequency of 400 MHz. Throughput depends on the codes and how they are mixed and the actual clock frequency on the device.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Zynq® UltraScale+™ MPSoC, UltraScale™, UltraScale+™, 7 Series
Supported User Interfaces	AXI4-Lite, AXI4-Stream
Provided with Core	
Design Files	N/A
Example Design	IP Integrator Block Diagram
Test Bench	Verilog
Constraints File	Not Provided
Simulation Model	System Verilog Secure model Bit-accurate C model MEX file for use with MATLAB
Supported S/W Driver	Standalone
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

- Less than **20% of future space qualified F¨PGA** (LUTs - few BRAMs), **assuming strong derating (50%)** on fMAX (200 MHz)
- These results **can be optimized** to increase the throughput/area of LDPC serial-parallel encoders.



- About **560k LUTs and 833 BRAMs** assuming strong derating (50%) on fMAX (250 MHz)
- Can be **easily achieved on several high-end FPGA** technologies (Xilinx, Intel)

Part 2 – 10Gbit/s uplink

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Low on board resources consumption

In-house design LDPC assuming hard inputs (No ADC on board the satellite)

- **Regular LDPC**
- **Optimization of hard input decoder to save power consumption on board**

R	OOK 10 Gbit/s
1/2	1,32
4/5	0,82

Power gap wrt to capacity [dB]

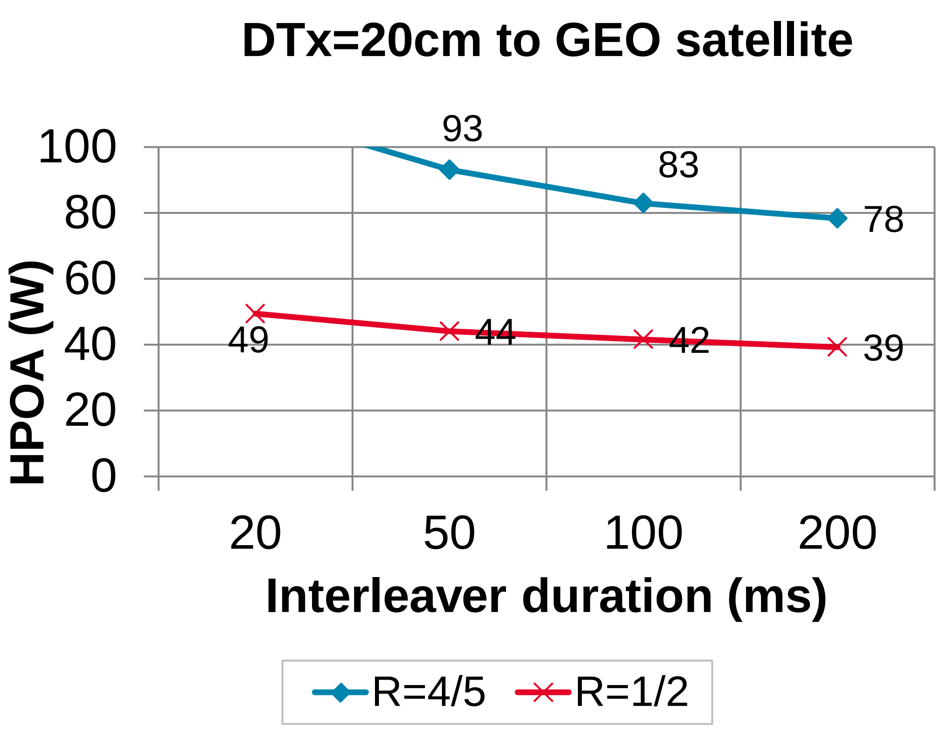
	Flip-Flop	LUT6	Bloc RAM
LDPC (20480, 16384) R =4/5		< 20%	
LDPC (32768, 16384) R= 1/2			

Occupancy percentage of space qualified FPGA

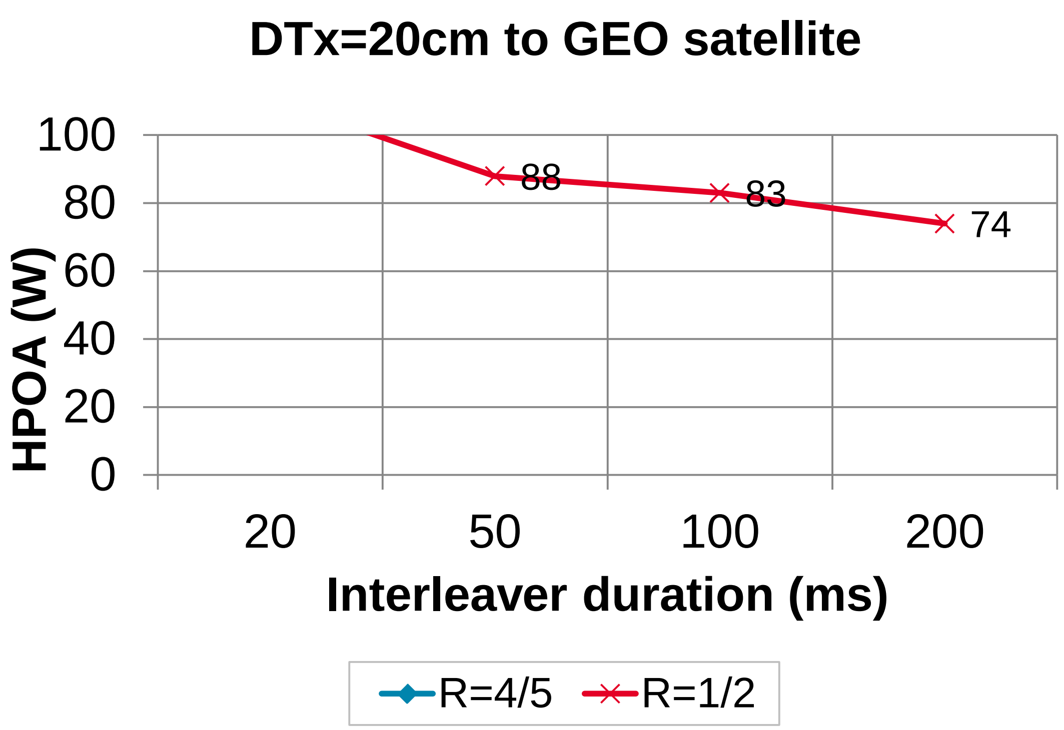
Good performances and low on-board consumption is reached nevertheless…

Optical uplink to GEO satellite

70% of the time it should be liked this or better…



Some time it could be liked this or worst…



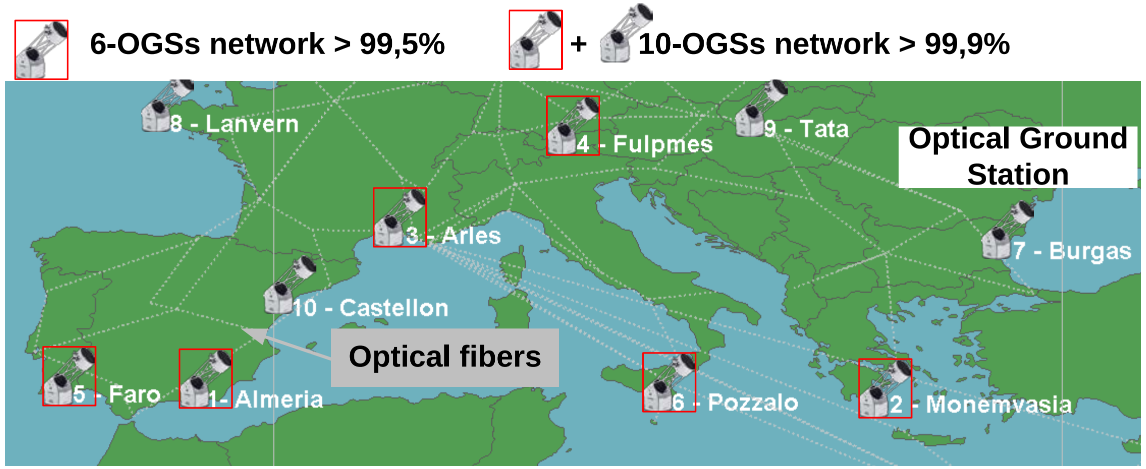
Error free uplink is power consuming

Conclusion

The lack of extensive characterization of Cn^2 profile for sites « relevant » for broadband satellite system shall be solved.

All affordable « CAPEX but also OPEX » techniques to make uplink easier is nice to have.

We perform simulations to estimate the interest of technologies on the end-to-end system.



Thank you