FORTRESS 2017

1st International Workshop on **For**mal **T**echniques for **Re**al-Time **S**ystem**s**

Satellite workshop of 23rd IEEE International Conference on Embedded and Real-Time Computing Systems and Applications

Hsinchu, Taiwan, 16-18th August 2017

Conference web site: www.rtcsa.org

IMPORTANT DATES

Paper submission deadline:	~~31 May, 2017~~ **extended to 18 June, 2017**
Notification of acceptance:	**1 July, 2017**
Final paper submission:	7 July, 2017
Workshop:	16 August, 2017

CALL FOR PAPERS

Many are the works proposed on timing and schedulability analysis for guaranteeing the predictability of single- and multi-core systems. The increasing complexity of embedded and real-time systems requires a continuous development in design and verification.

Formal methods are mathematics-based techniques for the specification, development and verification of software and hardware systems. In a certification context, industrials are more and more encouraged to apply formal methods such as model checking, abstract interpretation, etc. to guarantee the fulfillment of system requirements.

Applied to real-time, formal methods can be used to model real-time task behaviors, model task interactions and encode real-time requirements/properties such as timing constraints. They bring formal verification to timing and schedulability analysis of embedded and real-time systems.

The Formal Techniques for Real-Time Systems (FORTRESS) workshop provides a venue for bringing together researchers and developers from academia and industry to promote cross-fertilization and discuss advances dealing with the application of formal methods to embedded and real-time systems. Of particular interest are ideas and contributions that present significant paradigm shifts, explore unique and unconventional approaches to important problems, or investigate fundamental departures from conventional wisdom in adopted solutions.

SCOPE

The goal of the FORTRESS workshop is to provide an overview over the current research in formal methods applied to embedded and real-time systems.

Suggested topics of interest include (but are not restricted to):

- formal methods (SAT-/SMT-based techniques, model checking, static analysis, etc.) for timing and schedulability analysis

- formal techniques for the design of embedded and real-time systems

- development of correct real-time systems

- verification and validation of embedded and real-time systems

- simulation-based validation and verification

- runtime verification of real-time systems

SUBMISSIONS

Both research and industry papers are solicited. The submitted manuscript must describe original work not previously published and not concurrently submitted elsewhere. Submissions should be no more than 8 pages in the IEEE conference proceedings format (two-column, single-space, 10pt). The prospective authors should submit their papers through the submission

Authors of accepted papers agree to attend the workshop and to present their work during the workshop.

WORKSHOP CO-CHAIRS

Julien Brunel, ONERA Toulouse
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PROGRAM COMMITTEE

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